PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	)	
	)	
DAISABURO TAKASHIMA	)	GROUP ART UNIT: 2818
	)	
DIV. OF SERIAL NO.: 10/607,301	)	EXAMINER: L. PHAM
	)	
FILED: HEREWITH	)	
	)	
FOR: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING FERROELECTRIC CAPACITORS	)	ATTY. DKT. NO. 01701.00204

INFORMATION DISCLOSURE STATEMENT

Commission for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with Applicants' duty of disclosure, the enclosed information is submitted to the United States Patent and Trademark Office in connection with the above-identified application. The information is identified on the attached PTO Form-1449.

This application relies, under 35 U.S.C. §120, on the earlier filing date of prior U.S. Application Serial Nos. 10/607,301 filed June 27, 2003, 10/279, 910 filed on October 25, 2002 and 09/902,168 filed on July 11, 2001. The references identified on the attached Form PTO 1449 were submitted to and/or cited by the Patent and Trademark Office in these prior applications and, therefore, copies are not required to be provided in this application. See 37 C.F.R. Section 1.98(d).

Applicant does not waive any right to take appropriate action to establish patentability over the listed documents should they be applied as references against the claims of the present

application.

It is respectfully requested that the Examiner fully consider each of the documents, initial the enclosed Form PTO-1449 in the appropriate place to indicate that the document has been considered, and return a copy of the initialed form to the undersigned in accordance with MPEP Section 609.

Respectfully submitted,

By: _____

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Dated: March 17, 2004

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 01701.00204	SERIAL NUMBER Div. of 10/607,301
	APPLICANT Takashima	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE Herewith	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	6,459,118 B1	10/02	Kang			
	6,320,783 B1	11/01	Kang et al.			
	6,088,286	7/00	Yamauchi et al.			
	5,903,492	5/11/99	Takashima			
	5,894,447 A	04/99	Takashima			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	K. Noda et al., "A Boosted Dual Word-line Decoding Scheme for 256Mb DRAMs" Symposium on VLSI Circuits Digest of Technical Papers; pp. 112-113; 1992.
	M. Nakamura et al., "A 29ns 64Mb DRAM with Hierarchical Array Architecture" IEEE International Solid-State Circuits Conference, pp. 246-247, 1995.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.